WHAT IS CLAIMED IS:

1. A method for fabricating a metal oxide semiconductor field effect transistor (MOSFET) comprising the steps of:

providing a substrate having spaced apart source and drain regions on the substrate with the space between the source and drain regions defining a channel region;

forming a dielectric layer peripherally about the drain portion to completely surround the drain region and in contact with the source region to fill the channel region, wherein the area of the dielectric layer in the channel region between the drain and source regions is variable in length; and,

forming a gate electrode layer on at least a portion of the dielectric layer in the channel region.

2. The method of Claim 1, wherein the substrate is a layer of mono-crystalline silicon, the dielectric layer is silicon dioxide and the gate electrode layer is poly-crystalline silicon.

3. The method of Claim 1, wherein a width-length ratio of the transistor is less than or equal to unity

4. The method of Claim 2, wherein a width-length ratio of the transistor is less than or equal to unity.

5. The method of Claim 1, wherein the source and drain regions are doped oppositely to said channel region.

6. The method of Claim 1, wherein the source and drain regions are interchangeable.

7. The method of Claim 1, wherein step of forming the gate electrode layer includes covering the entire portion of the dielectric layer in the channel region.

8. The method of Claim 2, wherein step of forming the gate electrode layer includes covering the entire portion of the dielectric layer in the channel region.

9. The method of Claim 1, wherein step of forming the gate electrode layer includes forming the gate electrode layer peripherally about the dielectric layer and covering the portion of the dielectric layer in the channel region.

10. A metal oxide semiconductor field effect transistor (MOSFET) having a substrate, comprising:

spaced apart source and drain regions on the substrate with the space between the source and drain regions defining a channel region;

a dielectric layer peripherally about the drain region to completely surround the drain region and filling the channel region such that the dielectric layer is in contact with the source region, wherein the area of the dielectric layer in the channel region between the drain and source regions is variable in length; and,

a gate electrode layer covering at least a portion of the dielectric layer in the channel region.

11. The MOSFET of Claim 10, wherein the substrate is a layer of mono-crystalline silicon, the dielectric layer is silicon dioxide and the gate electrode layer is poly-crystalline silicon.

12. The MOSFET of Claim 10, wherein a width-length ratio of the transistor is less than or equal to unity.

13. The MOSFET of Claim 11, wherein a width-length ratio of the transistor is less than or equal to unity.

14. The MOSFET of Claim 10, wherein the source and drain regions are doped oppositely to a channel region.

15. The MOSFET of Claim 10, wherein said source and drain regions are interchangeable.

16. The MOSFET of Claim 10, wherein the gate electrode layer covers the portion of the dielectric layer in the channel region.

17. The MOSFET of Claim 11, wherein the gate electrode layer covers the portion of the dielectric layer in the channel region.

18. The MOSFET of Claim 10, wherein the gate electrode layer is peripherally about the dielectric layer and covers the portion of the dielectric layer in the channel region.